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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,344	11/24/2003	Robert Gentile	500219.02	4725

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Kimton N. Eng, Esq.
DORSEY & WHITNEY LLP
Suite 3400
1420 Fifth Avenue
Seattle, WA 98101

EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,344	GENTILE ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 32-83 of U.S. Application 10/722,344 are currently pending.
2. The application was filed on 5/24/2004.
3. The application is a continuation of U.S. Application 09/083,959, filed on May 22,1998 (now U.S. Patent 6,654,714).

Information Disclosure Statement

4. The "OpenVMS DCL Dictionary" was not found in the parent application. Examiner was unable to locate a copy by other means. Applicants are requested to provide a copy for the instant application.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. The prior art used for these rejections is as follows:

    a. Intel MultiProcessor Specification. Version 1.4. May 1997. © 1993-1997. ("**Intel**").

    b. Ghori et al., U.S. Patent 5,884,091. (Hereinafter "**Ghori**").

7. **Claims 32-35, 37-44, 46-56, 58-66, and 68-83 are rejected under 35 U.S.C. 102(b) as being anticipated by Intel.**

8. The following discussion of the Intel reference applies to all claims.

9. Intel teaches a Multiprocessor (MP) System Architecture (see Fig.2-1 on p.2-1).

10. Intel also specifically teaches: "While all processors in a complaint system are functionally identical, this specification classifies them into two types: the bootstrap processor (BSP) and the application processors (AP). ... This differentiation is for convenience and is in effect only during the initialization and shutdown processes. The BSP is responsible for initializing the system and booting the operating system; APs are activated only after the system is up and running." (see pp.2-2 to 2-3).

11. Intel also specifically teaches: "The operating system must have access to some information about the multiprocessor configuration. The MP specification teaches two methods for passing this information to the operating system ..." (see p.4-1).

12. Intel also teaches: "The following two data structures are used: (1) The Floating Pointer Structure ... (2) The MP Configuration Table ..." (see p.4-2). Examiner interprets that the MP Configuration Table corresponds to the claimed invention.

13. Intel also teaches: "The following is a list of the suggested memory spaces for the MP configuration table: (a) In the first kilobyte of Extended BIOS Data Area (EBDA), or (b) Within the last kilobyte of system base memory if the EBDA segment is undefined, or (c) At the top of system physical memory, or (d) In the BIOS read-only memory space between 0E0000h and 0FFFFFh." (see p.4-2). Examiner interprets that "(b) Within the last kilobyte of system base memory" can be located on a "remote computer", as claimed in some of the dependent claims.

14. Intel teaches that the MP Configuration Table includes processor entries (see Table 4-3 on p.4-7), and shows the format of each processor entry (see Fig.4-4 on p.4-7), as well as defining the fields of each processor entry (see Table 4-4 on p.4-8).

15. Intel also teaches that the each processor entry includes a field for "CPUID Feature Flags" (see Table 4-4 on p.4-8). Intel also teaches that one of these flags is for support for the Intel387 floating point instruction set (see Table 4-6 on p.4-9). Each processor entry also includes a field for use of Intel CPU signatures (see Table 4-4 on p.4-8, and Table 4-5 on p.4-9).

16. Intel also teaches that the BSP boots the entire system by accessing the MP configuration table in order to send "wakeup" commands to the APs. (See pp.B-1 to B-3).

17. Finally, Intel teaches: "Some MP operating systems that exist today do not support processors of different types, speeds, or capabilities. However, as processor lifetimes increase and new generations of processors arrive, the

potential for dissimilarity among processors increases. The MP specification addresses this potential by providing an MP configuration table to help the operating system configure itself. Operating system writers should factor in processor variations, such as processor type, family, model, and features, to arrive at a configuration that maximizes overall system performance. At a minimum, the MP operating system should remain operational and should support the common features of unequal processors." (See p.B-7)

18. In regards Claim 32, Intel teaches the following limitations:

> *32. (New) A method of selecting a compatible processor for addition to a multiprocessor computer, the multiprocessor computer having at least one current processor and having at least one additional location in which a new processor can be added, the method comprising:*
>
> *executing a computer program on the multiprocessor computer*

(See Intel, especially: Fig.2-1 on p.2-1; and pp.2-2 to 2-3)

> *directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;*

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

> *obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;*

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

> *executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor; and*

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

19. Dependent Claims 33-35 and 37-39 are rejected on the same grounds as Independent claim 32.

20. In regards Claim 40, Intel teaches the following limitations:

40. (New) A method of selecting a compatible processor for addition to a multiprocessor computer, the multiprocessor computer having at least one current processor and having at least one additional location in which a new processor can be added, the method comprising:

executing a computer program on the multiprocessor computer

(See Intel, especially: Fig.2-1 on p.2-1; and pp.2-2 to 2-3)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer;

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible

with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor; and

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

21. Dependent Claims 41-44 and 46-49 are rejected on the same grounds as Independent claim 40.

22. In regards Claim 50, Intel teaches the following limitations:

50. (New) A system for selecting a new processor for addition to a multiprocessor computer having at least one current processor, the system comprising:

a first component on the multiprocessor computer that determines the identity of each current processor in the multiprocessor computer;

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

a second component that stores processor compatibility information indicative of processors that are compatible with a plurality of processors that includes each current processor;

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

a third component coupled to the first and second components to accesses the processor compatibility information using the identity of each current processor in the multiprocessor computer to determine the processors that are compatible with the at least one current processor; and

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

a fourth component coupled to the third component that provides information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

23. Dependent Claims 51-56 and 58-59 are rejected on the same grounds as Independent claim 50.

24. In regards Claim 60, Intel teaches the following limitations:

> *60. (New) A system for selecting a new processor for addition to a multiprocessor computer containing at least one current processor, the system comprising:*
>
> *a first component on the multiprocessor computer that determines the identity of each current processor in the multiprocessor computer;*

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

> *a second component allowing identifying information to be provided that identifies the new processor before adding the new processor to the multiprocessor computer;*

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

> *a third component that stores processor compatibility information indicative of processors that are compatible with a plurality of processors that includes each current processor;*

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

> *a fourth component coupled to the first, second and third components to compare the identifying information for the new processor with the compatibility information to, determine processors that are compatible with each current processor; and*

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

> *a fifth component that provides an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.*

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

25. Dependent Claims 61-66 and 68-69 are rejected on the same grounds as Independent Claim 60.

26. In regards Claim 70, Intel teaches the following limitations:

> *70. (New) A computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor, by:*
>
> *executing a computer program on the multiprocessor computer*

(See Intel, especially:)

> *directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;*

(See Intel, especially:)

> *obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;*

(See Intel, especially:)

> *executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor; and*

(See Intel, especially:)

> *providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.*

(See Intel, especially:)

27. Dependent Claims 71-75 are rejected on the same grounds as Independent Claim 70.

28. In regards Claim 76, Intel teaches the following limitations:

> *76. (New) A computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor, by:*
>
> *executing a computer program on the multiprocessor computer*

(See Intel, especially:)

> *directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;*

(See Intel, especially:)

> *obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;*

(See Intel, especially:)

> *providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer;*

(See Intel, especially:)

> *executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor; and*

(See Intel, especially:)

> *providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.*

(See Intel, especially:)

29. Dependent Claims 77-83 are rejected on the same grounds as Independent Claim 76.

30. Claims 32, 40, 50, 60, 70, and 76 are rejected under 35 U.S.C. 102(e) as being anticipated by Ghori.

31. In regards Claim 32, Ghori teaches the following limitations:

32. (New) A method of selecting a compatible processor for addition to a multiprocessor computer, the multiprocessor computer having at least one current processor and having at least one additional location in which a new processor can be added, the method comprising:

executing a computer program on the multiprocessor computer

(See Ghori, especially: col.3, line 63 to col.4, line 6; and col.5, lines 14-21)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a.)

providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

32. In regards Claim 40, Ghori teaches the following limitations:

40. (New) A method of selecting a compatible processor for addition to a multiprocessor computer, the multiprocessor computer having at least one current processor and having at least one additional location in which a new processor can be added, the method comprising:

executing a computer program on the multiprocessor computer

(See Ghori, especially: col.3, line 63 to col.4, line 6; and col.5, lines 14-21)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer;

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible

with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a.)

providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

33. In regards Claim 50, Ghori teaches the following limitations:

50. (New) A system for selecting a new processor for addition to a multiprocessor computer having at least one current processor, the system comprising:

a first component on the multiprocessor computer that determines the identity of each current processor in the multiprocessor computer;

(See Ghori, especially: col.3, line 63 to col.4, line 6;
and col.5, lines 14-54)

a second component that stores processor compatibility information indicative of processors that are compatible with a plurality of processors that includes each current processor;

(See Ghori, especially: Fig.3, and associated text at col.4, lines 62-66)

a third component coupled to the first and second components to accesses the processor compatibility information using the identity of each current processor in the multiprocessor computer to determine the processors that are compatible with the at least one current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.3, and associated text at col.4, lines 62-66)

a fourth component coupled to the third component that provides information identifying the processors that are compatible with each

current processor before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

34. In regards Claim 60, Ghori teaches the following limitations:

60. (New) A system for selecting a new processor for addition to a multiprocessor computer containing at least one current processor, the system comprising:

a first component on the multiprocessor computer that determines the identity of each current processor in the multiprocessor computer;

(See Ghori, especially: col.3, line 63 to col.4, line 6;
and col.5, lines 14-54)

a second component allowing identifying information to be provided that identities the new processor before adding the new processor to the multiprocessor computer;

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

a third component that stores processor compatibility information indicative of processors that are compatible with a plurality of processors that includes each current processor;

(See Ghori, especially: col.5, lines 29-54; and Fig.3, and associated text at col.4, lines 62-66)

a fourth component coupled to the first, second and third components to compare the identifying information for the new processor with the compatibility information to, determine processors that are compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.3, and associated text at col.4, lines 62-66)

a fifth component that provides an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

35. In regards Claim 70, Ghori teaches the following limitations:

70. (New) A computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor, by:

executing a computer program on the multiprocessor computer

(See Ghori, especially: col.3, line 63 to col.4, line 6; and col.5, lines 14-21)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a.)

providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

36. In regards Claim 76, Ghori teaches the following limitations:

76. (New) A computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor, by:

executing a computer program on the multiprocessor computer

(See Ghori, especially: col.3, line 63 to col.4, line 6; and col.5, lines 14-21)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer;

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a.)

providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

Claim Rejections - 35 USC § 103

37. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

38. The prior art used for these rejections is as follows:

a. Intel MultiProcessor Specification. Version 1.4. May 1997. © 1993-1997. ("**Intel**").

b. Official Notice

39. **Claims 36, 45, 57, and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel in view of Official Notice.**

40. In regards Claim 36, Ghori teaches the following limitations:

36. (New) The method of claim 33 wherein the computer that is remote from the multiprocessor computer is connected to the multiprocessor computer system via the Internet.

Intel teaches a Multiprocessor (MP) System Architecture (see Fig.2-1 on p.2-1). Intel also specifically teaches: "While all processors in a complaint system are functionally identical, this specification classifies them into two types: the bootstrap processor (BSP) and the application processors (AP). ... This differentiation is for convenience and is in effect only during the initialization and shutdown processes. The BSP is responsible for initializing the system and booting the operating system; APs are activated only after the system is up and running." (see pp.2-2 to 2-3).

Intel, however, does not expressly teach that the AP computers are connected to the BSP computer via the Internet. Official Notice is given that this practice was old and well known at the time the invention was made.

41. Claims 45, 57, and 67 are rejected on the same grounds as claim 36.

Conclusion

42. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

43. U.S. Patent 5,490,279 to Golbert et al. (Teaches a method and apparatus for operating a single CPU computer system as a multiprocessor system).

44. U.S. Patent 5,884,091 to Zalewski et al. (Priority date of 11/4/1997. See especially col.21, lines 21-30, which teaches the "need to recognize other CPUs that are not compatible").

45. U.S. PG-PUB 2004/0193861 to Michaelis. (Too recent to be applied as prior art. Note claim 20).

46. Mazur, G. "Identification of 32-bit x86 CPUs Based on Reset Signature." © 1996. Last update: 9/11/2000. http://graf.ii.pw.edu.pl/gbm/x86/reset.html. (Teaches a non-CPUID method of recognizing a CPU).

47. Mazur, G. "Identification of 486-class CPUs; checking for CPUID Support." © 1996-2000. Last update: 5/20/2000. http://graf.ii.pw.edu.pl/gbm/x86/base486.html (Teaches the CPUID method of recognizing a 486-class CPU).

48. Mazur, G. "Identification of x86 CPUs with CPUID Support." © 1996-2000. Last update: 9/29/2000. http://graf.ii.pw.edu.pl/gbm/x86/cpuid.html (Teaches the CPUID method of recognizing an x86 CPU).

49. Steunebrink, J. "CPU Upgrade: How to Easily Check Your CPU Vendor, Model, Internal Speed, and L1 Cache Mode Settings." © 1997-2006. Last update: 7/7/2006. http://web.inter.nl.net/hcc/J.Steunebrink/chkcpu.htm.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is

(571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a bi-week, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753.

Any response to this office action should be faxed to (571) 273-8300, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
July 27, 2006

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100